IN THE SPECIFICATION:

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] United States Patent 4,862,245 to Pashby illustrates a "leads-over-chip" (LOC) configuration, wherein the inner lead ends of a standard dual-in-line package (DIP) lead frame configuration extend over and are secured to the active (upper) surface of the semiconductor device through a dielectric layer. The bond wire length is shortened by placing the inner lead ends in closer proximity to a central row of die bond pads, and the lead extensions purportedly enhance heat transfer from the semiconductor device. However, the Pashby LOC configuration, as disclosed, relates to mounting and bonding a single semiconductor device with the inner lead ends of the lead fingers to the surface of the semiconductor device.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] Fig. 2 is a ~~cross-sectional~~ cross-sectional view taken along line A-A of Fig. 1 of a portion of the semiconductor assembly of the first embodiment of the present invention;